Process Flow Specification rev 0.9c 1/21/2004

This documents the process through which a potential language enhancement request becomes a proposal from the BTF (Behavioral Task Force) or any Task Force to the VSG (1364 Verilog Standard working Group). The purpose of this specification is to ensure that there is a simple well-documented process through which a technology donation or enhancement request flows before becoming a part of the draft standard.
The scope of this specification is from donation/request through presentation to the VSG. It is intended as a simple how-to guide and does not set new guidelines, by-laws or rules.

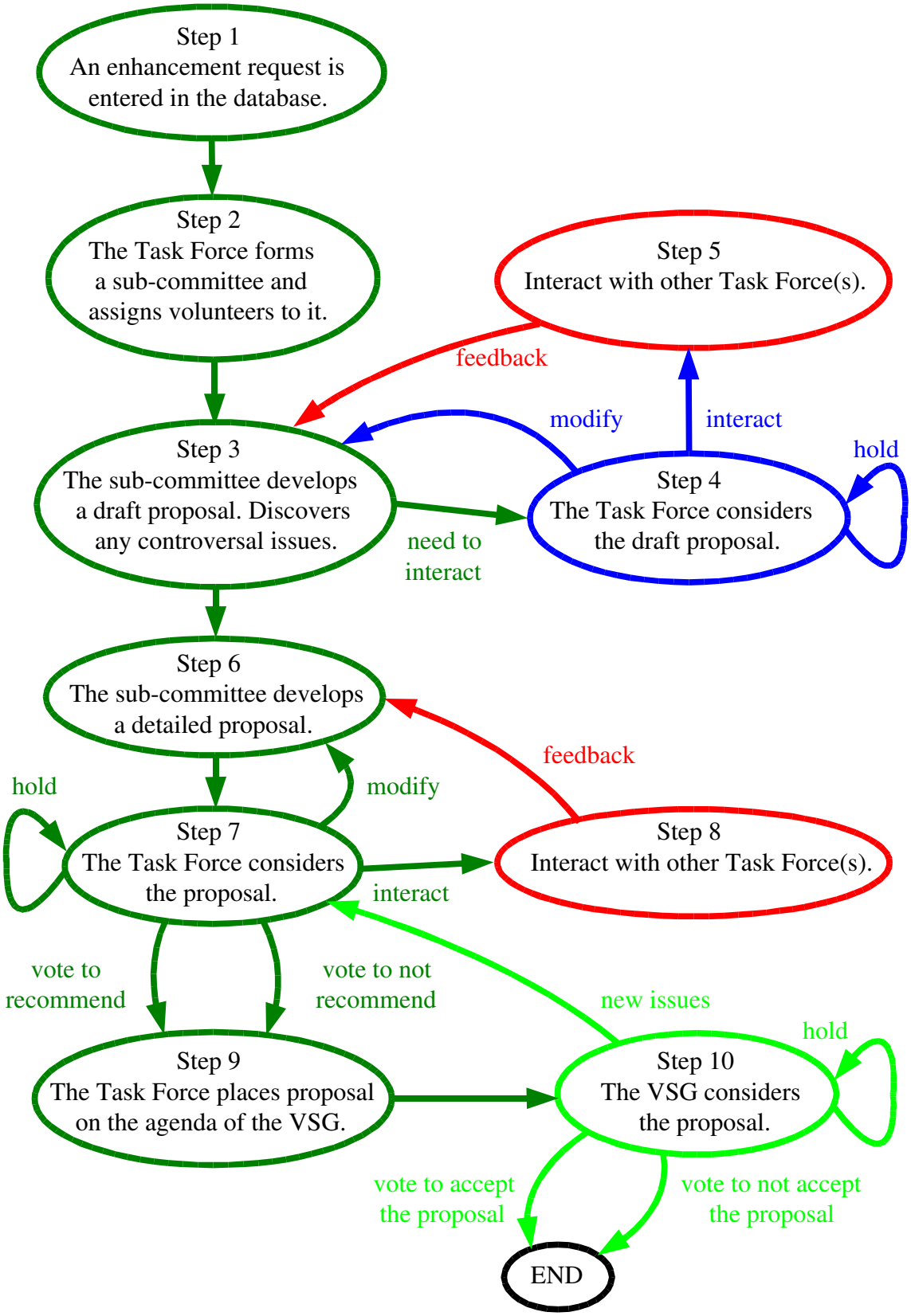
Why?

In theory, at a VSG meeting an enhancement request could be discussed and have words created for it (i.e. a proposal) and be adopted into the new draft of the Verilog Standard.
However, this rarely, if ever, happens. Usually a small number of members are intensely interested in the enhancement, and they are involved in a time-consuming discussion of the technical details of the enhancement's proposal and are asked by the rest of the members of the VSG to meet and reach consensus outside the VSG meeting.

Because of this inherent conflict over the length of discussion of the technical issues associated with the development of an enhancements proposal, a process was needed to keep discussion of technical details in small focused groups/meetings.

This process is not trying to limit good technical discussion. This process intends to optimize the effective use of all members' time. To that end, the VSG has partitioned responsibilities to task forces (subgroups) of the VSG. The BTF (Behavioral Task Force) itself recognizes the inefficiencies associated with this inherent conflict over the length of discussion of the technical issues and as a result has developed this process flow guideline. This process helps to make the discussion of technical issues available to those who are most interested/concerned with them. Thus most of this discussion can take place before the proposal reaches the VSG.

This document is intended to provide an explanation for the process flow whereby an enhancement request becomes part of the new draft of Verilog Standard. This document is not a set of rules, it is a guideline, the VSG and BTF are free to make exceptions at any time.


Step 1
An enhancement request is entered in the database.
Step 2
The Task Force forms a sub-committee and assigns volunteers to it.
Step 3
The sub-committee develops a draft proposal. Discovers any controversal issues.
Step 4
The Task Force considers the draft proposal.
Step 5
Interact with other Task Force(s).
feedback
modify
interact
hold
need to interact
Step 6
The sub-committee develops a detailed proposal.
Step 7
The Task Force considers the proposal.
Step 8
Interact with other Task Force(s).
feedback
hold
modify
interact
vote to recommend
vote to not recommend
Step 9
The Task Force places proposal on the agenda of the VSG.
Step 10
The VSG considers the proposal.
new issues
hold
vote to accept the proposal
vote to not accept the proposal
END

Step 1.

An enhancement request should be or has been entered into the enhancements database. This enhancement request might either come from a user with no donation associated with it or come from a CAD vendor/developer and have a donation attached to it.
Advance to step 2.

Step 2.

The Task Force will assign a volunteer (read "champion") and/or make a sub-committee and assign volunteers to an enhancement request.
Advance to step 3.

Step 3.

The champion and/or sub-committee will develop a draft proposal for this enhancement request. The technical issues of any controversy need to be discovered. Start saving emails on the reflectors concerning these said technical issues. Also start filling out a copy of the Proposal Evaluation Template and save in the database.

A: If interactions with other Task Force(s) on issues related to the proposal are needed then. Advance to step 4.

B: Procede to step 6.

Step 4.

The Task Force considers the draft proposal. The Task Force may:

A: Raise new issues which need addressing, and returns the proposal to the champion and/or sub-committee, maybe with a request to the champion and/or subcommittee to improve, modify or rewrite. Return to step 3.

B: Sees the need to interact with other Task Force(s) on these issues.
Send to step 5.

C: Table the draft proposal till a later date. Hold at step 4.
(if the draft proposal is tabled, it maybe looked at in the next meeting, or it might be tabled indefinitely.)

Step 5.

Interface/interact with other Task Force(s) to get feedback for the champion and/or subcommittee to improve, modify or rewrite.
Return to step 3.

Step 6.

The champion and/or sub-committee will finish the development of a detailed proposal for this enhancement request. A fleshed out proposal includes an overview, exact wording of changes to the draft of 1364 Verilog Standard, and technical reasoning and rationale behind anything of any controversy. Also saved in the enhancement database is the probable exchange of emails on the reflectors concerning said technical reasoning and rationale behind any issues. Also a copy of the Proposal Evaluation Template will be filled out as completely as possible and saved in the database.
Advance to step 7.

Step 7.

The Task Force considers the proposal. The Task Force may:

A: Raise new issues which need addressing, and returns the proposal to the champion and/or sub-committee, maybe with a request to the champion and/or subcommittee to improve, modify or rewrite. Return to step 6.

B: Raise the need, perhaps pointed out by the Proposal Evaluation Template to interact with other Task Force(s) on issues related to the proposal.
Send to step 8.

C: Table the proposal till a later date. Hold at step 7.

D: Vote to not recommend. Advance to step 9.

E: Vote to recommend . Advance to step 9.

Step 8.

Interface/interact with other Task Force(s) to get feedback for the champion and/or subcommittee to improve, modify or rewrite.
Return to step 6.

Step 9.

The Task Force places proposal on the agenda of the VSG.

Step 10.

The proposal is presented to the VSG by the Task Force with a recommendation in favor or against. The VSG may:

A: Raise new issues which need addressing, and returns the proposal to the Task Force. Return to step 7.

B: Table the proposal till a later date. Hold at step 10.

C: Vote to not accept the proposal. END.

D: Vote to accept the proposal into the draft of 1364 Verilog Standard. END.

This process flow is a written document of the ad hoc procedure developed during the years of work on the 2001 version of the standard including some number of changes and modifications. This document attempts to codify these unwritten guidelines.

Again remember that this process flow document is not a set of rules, it is a guideline, the working group and task forces are free to make exceptions at any time.